Fifth Semester					
Group	**Paper Code**	**Paper**	**L**	**P**	**Credits**
Theory Papers					
HS/MS	HS-301	Economics for Engineers	2		2
PC	ECC-303	Digital Signal Processing	4		4
PC	ECC-305	Microelectronics	3		3
PC	EEC-307	Introduction to Control Systems	3		3
PC	ECC-309	Transmission Lines, Waveguides and Antenna Design	4		4
PC	ECC-311	Data Communication and Networking	4		4
Practical / Viva Voce					
PC	ECC-351	Digital Signal Processing Lab		2	1
PC	ECC-353	Microelectronics Lab		2	1
PC	EEC-355	Introduction to Control Systems Lab		2	1
PC	ECC-357	Transmission Lines, Waveguides and Antenna Design Lab		2	1
PC	ECC-359	Data Communication and Networking Lab		2	1
PC / Internship	ES-361	Summer Training Report - 1 *			1
Total		_	**20**	**10**	**26**

***NUES:**Comprehensive evaluation of the Summer Training Report – 1 (after 4th Semester) shall be done by the committee of teachers, constituted by the Academic Programme Committee, out of 100. The training shall be of 4 to 6 weeks duration. The training can be under the mentorship of a teacher of the institute.

Sixth Semester					
Group	**Paper Code**	**Paper**	**L**	**P**	**Credits**
Theory Papers					
HS/MS	MS-302	Principles of Management for Engineers	3		3
HS/MS	HS-304	Universal Human Values*	1		1
PCE		Programme Core Elective Paper (PCE –1)			4
PCE		Programme Core Elective Paper (PCE – 2)			4
PCE		Programme Core Elective Paper (PCE – 3)			4
EAE / OAE		Emerging Area/Open Area Elective Paper (EAE – 1 /OAE – 1)			4
EAE / OAE		Emerging Area/Open Area Elective Paper (EAE – 2 /OAE – 2)			4
Practical / Viva Voce					
HS/MS	HS-352	NSS / NCC / Cultural Clubs / Technical Society / Technical Club**			2
Total					**26**

***NUES:**All examinations to be conducted by the concerned teacher as specified in the detailed syllabus of the paper.

****NUES:** Comprehensive evaluation of the students by the concerned coordinator of NCC / NSS / Cultural Clubs / Technical Society / Technical Clubs, out of 100 as per the evaluation schemes worked out by these activity societies, organizations; the faculty co-ordinators shall be responsible for the evaluation of the same. These activities shall start from the 1st semester and the evaluation shall be conducted at the end of the 6th semester for students admitted in the first semester. Students admitted in the 2nd year (3rd semester) as lateral entry shall be evaluated on the basis their performance, by the faculty co-ordinator for the period of 3rd semester to 6th semester only.

Introduction to Control Systems Lab	L	P	C
		2	1

Discipline(s) / EAE / OAE	Semester	Group	Sub-group	Paper Code
ECE/EE/EEE/ICE/EE-VDT/ EC-ACT	5	PC	PC	EEC-355

Marking Scheme:
1. Teachers Continuous Evaluation: 40 marks
2. Term end Theory Examinations: 60 marks

Instructions:
1. The course objectives and course outcomes are identical to that of (Introduction to Control Systems) as this is the practical component of the corresponding theory paper.
2. The practical list shall be notified by the teacher in the first week of the class commencement under intimation to the office of the Head of Department / Institution in which the paper is being offered from the list of practicals below. Atleast 10 experiments must be performed by the students, they may be asked to do more. Atleast 5 experiments must be from the given list.

1. Determination of step & impulse response for a second-order unity feedback system.
2. To study the speed-torque characteristics of SERVO MOTOR.
3. Experiment to draw synchro pair characteristics.
4. To determine the Transfer Function of the DC Machine.
5. Plot unit step response of the given transfer function and finds delay time, rise time, and peak overshoot.
6. Plot the pole-zero configuration in the s-plane for the given transfer function.
7. To determine the characteristics of Magnetic Amplifiers.
8. Linear System Analysis (Time Domain Analysis, Error Analysis) Using MATLAB.
9. To observe the effect of P, PI, PID, and PD Controller for open loop and closed loop of second order system.
10. To analyze the frequency response of a system by plotting Root locus, Bode plot, and Nyquist plot using MATLAB software.
11. Experiment to draw the frequency response characteristics of the lag–lead compensator network and determination of its transfer function.
12. Temperature Controller Using PID Controller.
13. Study of operation of a stepper motor interface with a microprocessor.

Data Communication and Networking	L	P	C
	4		4

Discipline(s) / EAE / OAE	Semester	Group	Sub-group	Paper Code
ECE/EE-VDT/EC-ACT	5	PC	PC	ECC-311

Marking Scheme:
1. Teachers Continuous Evaluation: 25 marks
2. Term end Theory Examinations: 75 marks

Instructions for paper setter:
1. There should be 9 questions in the term end examinations question paper.
2. The first (1st) question should be compulsory and cover the entire syllabus. This question should be objective, single line answers or short answer type question of total 15 marks.
3. Apart from question 1 which is compulsory, rest of the paper shall consist of 4 units as per the syllabus. Every unit shall have two questions covering the corresponding unit of the syllabus. However, the student shall be asked to attempt only one of the two questions in the unit. Individual questions may contain upto 5 sub-parts / sub-questions. Each Unit shall have a marks weightage of 15.
4. The questions are to be framed keeping in view the learning outcomes of the course / paper. The standard / level of the questions to be asked should be at the level of the prescribed textbook.
5. The requirement of (scientific) calculators / log-tables / data – tables may be specified if required.

Course Objectives :

1.	To build an understanding of the fundamental concepts of data communication.
2.	To familiarize the student with the basic taxonomy of data link layer.
3.	To understand and implements the network routing, IP addressing, subnetting.
4.	To enumerate the functions of transport layer and application layer.

Course Outcomes (CO)

CO 1	Understand basic concepts of data communications.
CO 2	Understand and explain various functions of data link layerr.
CO 3	Understand and implements the network routing, IP addressing, subnetting.
CO 4	Enumerate the functions of transport layer and application layer.

Course Outcomes (CO) to Programme Outcomes (PO) mapping (scale 1: low, 2: Medium, 3: High)

	PO01	PO02	PO03	PO04	PO05	PO06	PO07	PO08	PO09	PO10	PO11	PO12
CO 1	3	2	1	1	3	1	-	-	-	-	-	3
CO 2	3	2	1	1	3	1	-	-	-	-	-	3
CO 3	3	2	1	1	3	1	-	-	-	-	-	3
CO 4	3	2	1	1	3	1	-	-	-	-	-	3

UNIT- I

Data Communications : Components, protocols and standards, Network and Protocol Architecture, Reference Model ISO-OSI, TCP/IP-Overview ,topology, transmission mode, digital signals, digital to digital encoding, digital data transmission, DTE-DCE interface, interface standards, modems, cable modem, transmission media-guided and unguided, transmission impairment, Performance, wavelength and Shannon capacity. Review of Error Detection and Correction codes.
Switching: Circuit switching (space-division, time division and space-time division), packet switching (virtual circuit and Datagram approach), message switching.

UNIT- II

Data Link Layer: Design issues, Data Link Control and Protocols: Flow and Error Control, Stop-and-wait ARQ. Sliding window protocol, Go-Back-N ARQ, Selective Repeat ARQ, HDLC, Point-to –Point Access: PPP Point –to-Point Protocol, PPP Stack

Medium Access Sub layer: Channel allocation problem, Controlled Access, Channelization, multiple access protocols, IEEE standard 802.3 & 802.11 for LANS and WLAN, high-speed LANs, Token ring, FDDI based LAN, Network Devices-repeaters, hubs, switches bridges.

UNIT- III

Network Layer: Design issues, Routing algorithms, Congestion control algorithms,
Host to Host Delivery: Internetworking, addressing and routing, IP addressing (class full & Classless), Subnet, Network Layer Protocols: ARP, IPV4, ICMP, IPV6 ad ICMPV6.

UNIT- IV

Transport Layer: Process to Process Delivery: UDP; TCP, congestion control and Quality of service.
Application Layer: Client Server Model, Socket Interface, Domain Name System (DNS): Electronic Mail (SMTP), file transfer (FTP), HTTP and WWW.

Text Books:

1. A. S. Tannenbum, D. Wetherall, "Computer Networks", Prentice Hall, Pearson, 5th Ed
2. Behrouz A. Forouzan, "Data Communications and Networking", Tata McGraw-Hill, 4th Ed

Reference Books:

1. Fred Halsall, "Computer Networks", Addison – Wesley Pub. Co. 1996.
2. Larry L, Peterson and Bruce S. Davie, "Computer Networks: A system Approach", Elsevier, 4th Ed
3. Tomasi, "Introduction To Data Communications & Networking", Pearson 7th impression 2011
4. William Stallings, "Data and Computer Communications", Prentice Hall, Imprint of Pearson, 9th Ed.
5. Zheng , "Network for Computer Scientists & Engineers", Oxford University Press
6. Data Communications and Networking: White, Cengage Learning

Data Communication and Networking Lab	L	P	C
		2	1

Discipline(s) / EAE / OAE	Semester	Group	Sub-group	Paper Code
ECE/EE-VDT/EC-ACT	5	PC	PC	ECC-359

Marking Scheme:
1. Teachers Continuous Evaluation: 40 marks
2. Term end Theory Examinations: 60 marks

Instructions:
1. The course objectives and course outcomes are identical to that of (Data Communication and Networking) as this is the practical component of the corresponding theory paper.
2. The practical list shall be notified by the teacher in the first week of the class commencement under intimation to the office of the Head of Department / Institution in which the paper is being offered from the list of practicals below. Atleast 10 experiments must be performed by the students, they may be asked to do more. Atleast 5 experiments must be from the given list.

1. Introduction to Computer Network laboratory
   Introduction to Discrete Event Simulation
   Discrete Event Simulation Tools - ns2/ns3, Omnet++
2. Using Free Open Source Software tools for network simulation – I Preliminary usage of the tool ns3
   Simulate telnet and ftp between N sources - N sinks (N = 1, 2, 3). Evaluate the effect of increasing data rate on congestion.
3. Using Free Open Source Software tools for network simulation - II
   Advanced usage of the tool ns3
   Simulating the effect of queueing disciplines on network performance - Random Early Detection/Weighted RED / Adaptive RED (This can be used as a lead up to DiffServ / IntServ later).
4. Using Free Open Source Software tools for network simulation - III
   Advanced usage of the tool ns3 Simulate http, ftp and DBMS access in networks
5. Using Free Open Source Software tools for network simulation - IV
   Advanced usage of the tool ns3
   Effect of VLAN on network performance - multiple VLANs and single router.
6. Using Free Open Source Software tools for network simulation - IV
   Advanced usage of the tool ns3
   Effect of VLAN on network performance - multiple VLANs with separate multiple routers.
7. Using Free Open Source Software tools for network simulation - V
   Advanced usage of the tool ns3
   Simulating the effect of DiffServ / IntServ in routers on throughput enhancement.
8. Using Free Open Source Software tools for network simulation - VI
   Advanced usage of the tool ns3
   Simulating the performance of wireless networks
9. Case Study I : Evaluating the effect of Network Components on Network Performance
   To Design and Implement LAN With Various Topologies and To Evaluate Network Performance Parameters for DBMS etc)
10. Case Study II : Evaluating the effect of Network Components on Network Performance
    To Design and Implement LAN Using Switch/Hub/Router As Interconnecting Devices For Two Different LANs and To Evaluate Network Performance Parameters.
11. Mini project - one experiment to be styled as a project of duration 1 month (the last month)

Digital Signal Processing Lab	L	P	C
		2	1

Discipline(s) / EAE / OAE	Semester	Group	Sub-group	Paper Code
ECE/ICE/EE-VDT/EC-ACT	5	PC	PC	ECC-351

Marking Scheme:
1. Teachers Continuous Evaluation: 40 marks
2. Term end Theory Examinations: 60 marks

Instructions:
1. The course objectives and course outcomes are identical to that of (Digital Signal Processing) as this is the practical component of the corresponding theory paper.
2. The practical list shall be notified by the teacher in the first week of the class commencement under intimation to the office of the Head of Department / Institution in which the paper is being offered from the list of practicals below. Atleast 10 experiments must be performed by the students, they may be asked to do more. Atleast 5 experiments must be from the given list.

1. Write Program to compute N point DFT of a given sequence and to plot magnitude and phase spectrum.
2. To implement Parseval theorem of DFT
3. To implement Time shifting and time reversal property of DFT
4. To find linear convolution of two given sequences.
5. To find circular convolution of two given sequences
6. To perform linear convolution from circular convolution and vice versa
7. To design LP FIR filter using windowing techniques
8. To design HP FIR filter using windowing techniques
9. To design LP IIR Butterworth filter for given specifications
10. To design LP IIR Chebyshev type-1 filter for given specifications
11. To verify the decimation of a given sequence
12. To verify the interpolation of a given sequence

Digital Systems Design	L	P	C
	3		3

Discipline(s) / EAE / OAE	Semester	Group	Sub-group	Paper Code
EEE	6	PCE	PCE-3	EEE-338T

Marking Scheme:

1. Teachers Continuous Evaluation: 25 marks
2. Term end Theory Examinations: 75 marks

Instructions for paper setter:

1. There should be 9 questions in the term end examinations question paper.
2. The first (1st) question should be compulsory and cover the entire syllabus. This question should be objective, single line answers or short answer type question of total 15 marks.
3. Apart from question 1 which is compulsory, rest of the paper shall consist of 4 units as per the syllabus. Every unit shall have two questions covering the corresponding unit of the syllabus. However, the student shall be asked to attempt only one of the two questions in the unit. Individual questions may contain upto 5 sub-parts / sub-questions. Each Unit shall have a marks weightage of 15.
4. The questions are to be framed keeping in view the learning outcomes of the course / paper. The standard / level of the questions to be asked should be at the level of the prescribed textbook.
5. The requirement of (scientific) calculators / log-tables / data – tables may be specified if required.

Course Objectives :

1.	To learn the basics of VHDL hardware
2.	To apply combinational logic circuits using VHDL
3.	To apply synchronous circuit using VHDL
4.	To apply asynchronous circuit using VHDL

Course Outcomes (CO)

CO 1	Understand the VHDL as a programming language
CO 2	Design combination logic circuit using VHDL
CO 3	Design sequential synchronous circuit using VHDL
CO 4	Design asynchronous circuit using VHDL

Course Outcomes (CO) to Programme Outcomes (PO) mapping (scale 1: low, 2: Medium, 3: High)

	PO01	PO02	PO03	PO04	PO05	PO06	PO07	PO08	PO09	PO10	PO11	PO12
CO 1	3	3	2	1	1	-	-	2	3	-	3	1
CO 2	1	2	2	2	-	3	-	2	-	-	-	-
CO 3	2	1	3	1	2	-	-	-	-	-	-	-
CO 4	1	1	2	2	-	-	-	-	-	-	-	-

UNIT I

Introduction to VHDL, design units, data objects, signal drivers, inertial and transport delays, delta delay, VHDL data types, concurrent and sequential statements. Subprograms – Functions, Procedures, attributes, generio, generate, package, IEEE standard logic library, file I/O, test bench, component declaration, instantiation, configuration**.**

UNIT II

Combinational logic circuit design and VHDL implementation of following circuits –first adder, Subtractor, decoder, encoder, multiplexer, ALU, barrel shifter, 4X4 key board encoder, multiplier, divider, Hamming code encoder and correction circuits.

UNIT III

Digital Signal Processing	L	P	C
	4		4

Discipline(s) / EAE / OAE	Semester	Group	Sub-group	Paper Code
ECE/ICE/EE-VDT/EC-ACT	5	PC	PC	ECC-303

Marking Scheme:
1. Teachers Continuous Evaluation: 25 marks
2. Term end Theory Examinations: 75 marks

Instructions for paper setter:
1. There should be 9 questions in the term end examinations question paper.
2. The first (1st) question should be compulsory and cover the entire syllabus. This question should be objective, single line answers or short answer type question of total 15 marks.
3. Apart from question 1 which is compulsory, rest of the paper shall consist of 4 units as per the syllabus. Every unit shall have two questions covering the corresponding unit of the syllabus. However, the student shall be asked to attempt only one of the two questions in the unit. Individual questions may contain upto 5 sub-parts / sub-questions. Each Unit shall have a marks weightage of 15.
4. The questions are to be framed keeping in view the learning outcomes of the course / paper. The standard / level of the questions to be asked should be at the level of the prescribed textbook.
5. The requirement of (scientific) calculators / log-tables / data – tables may be specified if required.

Course Objectives :

1.	To impart the basic knowledge of DFT, its properties, FFT and its applications.
2.	To impart the knowledge of designing and realization of FIR filters.
3.	To impart the knowledge of designing and realization of IIR filters.
4.	To impart the knowledge of quantization errors in Digital Signal Processing and the concept of Multirate signal processing.

Course Outcomes (CO)

CO 1	To understand the basic concept of DFT and FFT.
CO 2	To Acquire a clear idea of FIR filter designing techniques and realization methods.
CO 3	To understand the IIR filter designing techniques and realization methods and the stability.
CO 4	To understand the quantization errors in Digital Signal Processing and the concept of Multirate signal processing.

Course Outcomes (CO) to Programme Outcomes (PO) mapping (scale 1: low, 2: Medium, 3: High)

	PO01	PO02	PO03	PO04	PO05	PO06	PO07	PO08	PO09	PO10	PO11	PO12
CO 1	3	3	3	3	2	1	1	-	2	1	-	2
CO 2	3	3	3	3	2	1	1	-	2	1	-	2
CO 3	3	3	3	3	2	1	1	-	2	1	-	2
CO 4	3	3	3	3	2	1	1	-	2	1	-	2

UNIT I

Review of Discrete Time Fourier Transform, Z- transform and Discrete Fourier Transform, Properties of the DFT: Periodicity, Linearity and Symmetry properties, Multiplication of two DFTs, concept of circular convolution, computation of circular convolution by graphical and matrix form, relationship between linear convolution and circular convolution, computation of linear convolution from circular convolution, , linear filtering using DFT, aliasing error, filtering of long data sequences – Overlap-Save and Overlap-Add methods
Efficient computation of the DFT: Complexity analysis of direct computation of DFT, Concept of Fast Fourier transformation, Radix-2 computation of FFT using decimation-in-time and decimation-in-frequency algorithms, signal flow graphs, Butterflies, computations of FFT in one place using both algorithms, bit-reversal process, examples for DIT & DIF FFT Butterfly computations

UNIT II

Design & structure of FIR filters: Characteristics of practical frequency-selective filters, Basic concepts of IIR and FIR filters, Gibbs Phenomenon, Symmetric and Anti-symmetric FIR filters, Design of Linear-phase FIR filters using windows- Rectangular, Hamming, Hanning, Bartlett windows, FIR differentiator, FIR Hilbert Transformer. Design of FIR filters using frequency sampling method. Structure for FIR Systems: Direct form, Cascade form and Lattice structures.

UNIT III

Design & Structure of IIR filters: Concept of IIR digital filter, recursive and non-recursive system analog to digital domain transformation- Approximation of derivatives ,impulse invariant method and bilinear transformation and their properties, limitations of bilinear transformation, frequency warping and prewarping, methods to find out the order of IIR filter, mapping of poles and zeroes of filter in analog domain, computation of filter transfer function in analog domain, digital filter realization techniques, procedure to design Butterworth and Chebyshev digital IIR filters. Direct, Cascade, Parallel , Signal Flow graph and transposed structure, Lattice structures, Lattice and Lattice-Ladder Structures, Schur - Cohn stability Test for IIR filters

UNIT IV

Quantization Errors in Digital Signal Processing: Fixed point and floating point representation of numbers, Errors resulting from Rounding and Truncation, Digital Quantization of filter coefficients, Round-off effects in digital filters, Dead Band Effects.
Multirate Digital Signal Processing: Decimation, Interpolation, Sampling rate conversion by a rational factor; Frequency domain characterization of Interpolator and Decimator; Polyphase decomposition, Applications of Multirate signal processing.

Textbook(s):
1. Oppenheim & Schafer, Digital Signal Processing, PHI-latest edition.
2. Proakis and Manolakis, Digital Signal Processing, PHI Publication

Reference Books:
1. S. K. Mitra, Digital Signal Processing, TMH edition2006
2. Johny. R. Johnson, Introduction to Digital Signal Processing, PHI, Latest edition
3. R.Babu, Digital Signal Processing, Scitech Publication.

Economics for Engineers	L	P	C
	2		2

Discipline(s) / EAE / OAE	Semester	Group	Sub-group	Paper Code
All	5	HS/MS	HS	HS-301

Marking Scheme:
1. Teachers Continuous Evaluation: 25 marks
2. Term end Theory Examinations: 75 marks

Instructions for paper setter:
1. There should be 9 questions in the term end examinations question paper.
2. The first (1st) question should be compulsory and cover the entire syllabus. This question should be objective, single line answers or short answer type question of total 15 marks.
3. Apart from question 1 which is compulsory, rest of the paper shall consist of 4 units as per the syllabus. Every unit shall have two questions covering the corresponding unit of the syllabus. However, the student shall be asked to attempt only one of the two questions in the unit. Individual questions may contain upto 5 sub-parts / sub-questions. Each Unit shall have a marks weightage of 15.
4. The questions are to be framed keeping in view the learning outcomes of the course / paper. The standard / level of the questions to be asked should be at the level of the prescribed textbook.
5. The requirement of (scientific) calculators / log-tables / data – tables may be specified if required.

Course Objectives :

1.	To explain the basic micro and macro economics concepts.
2.	To analyze the theories of production, cost, profit and break even analysis.
3.	To evaluate the different market structures and their implications for thebehavior of the firm.
4.	To apply the basics of national income accounting and business cycles toIndian economy.

Course Outcomes (CO)

CO 1	Analyze the theories of demand, supply, elasticity and consumer choicein the market.
CO 2	Analyze the theories of production, cost, profit and break even analysis.
CO 3	Evaluate the different market structures and their implications for thebehavior of the firm.
CO 4	Apply the basics of national income accounting and business cycles toIndian economy.

Course Outcomes (CO) to Programme Outcomes (PO) mapping (scale 1: low, 2: Medium, 3: High)

	PO01	PO02	PO03	PO04	PO05	PO06	PO07	PO08	PO09	PO10	PO11	PO12
CO 1	1	2	1	2	1	-	1	-	1	1	3	1
CO 2	1	2	1	2	1	-	1	-	1	1	3	1
CO 3	1	2	1	2	1	-	1	-	1	1	3	1
CO 4	1	2	1	2	1	-	1	-	1	1	3	1

UNIT-I

Introduction: Economics Definition, Basic economic problems, Resource constraints and welfare maximization. Microand Macro economics. Production Possibility Curve.Circular flow of economic activities.
Basics of Demand, Supply and Equilibrium: Demand side and supply side of the market. Factors affecting demand & supply. Elasticity of demand & supply – price, income and cross-price elasticity. Market equilibrium price.

UNIT-II

Theory of Consumer Choice: Theory of Utility and consumer's equilibrium.Indifference Curve analysis, Budget Constraints, Consumer Equilibrium.
Demand forecasting: Regression Technique, Time-series, Smoothing Techniques: Exponential, Moving AveragesMethod

UNIT-III

Cost Theory and Analysis: Nature and types of cost, Cost functions- short run and long run, Economies and diseconomies of scale
Market Structure: Market structure and degree of competitionPerfect competition, Monopoly, Monopolistic competition, Oligopoly

UNIT - IV

National Income Accounting: Overview of Macroeconomics, Basic concepts of NationalIncome Accounting
Macro Economics Issues: Introduction to Business Cycle, Inflation-causes,consequences and remedies: Monetary and Fiscal policy.

Textbook(s):
1. H.C. Petersen, W.C. Lewis, Managerial Economics, 4th ed., Pearson Education 2001.

References:
1. S.K. Misra& V. K. Puri, Indian Economy, 38th ed., Himalaya Publishing House, 2020.
2. D.N. Dwivedi, Managerial Economics, 8th Edition, Vikas Publishing house
3. D. Salvatore, Managerial Economics in a Global Economy, 8th ed., Oxford University Press, 2015.
4. S. Damodaran, Managerial Economics, 2 nd ed., Oxford University Press, 2010.
5. M. Hirschey, Managerial Economics, 12th ed., Cengage India, 2013.
6. P.A. Samuelson, W.D. Nordhaus, S. Nordhaus,Economics,18th ed., Tata Mc-Graw Hill, 2006.

Introduction to Control Systems	L	P	C
	3		3

Discipline(s) / EAE / OAE	Semester	Group	Sub-group	Paper Code
ECE/EE/EEE/ICE/EE-VDT/ EC-ACT	5	PC	PC	EEC-307

Marking Scheme:

1. Teachers Continuous Evaluation: 25 marks
2. Term end Theory Examinations: 75 marks

Instructions for paper setter:

1. There should be 9 questions in the term end examinations question paper.
2. The first (1st) question should be compulsory and cover the entire syllabus. This question should be objective, single line answers or short answer type question of total 15 marks.
3. Apart from question 1 which is compulsory, rest of the paper shall consist of 4 units as per the syllabus. Every unit shall have two questions covering the corresponding unit of the syllabus. However, the student shall be asked to attempt only one of the two questions in the unit. Individual questions may contain upto 5 sub-parts / sub-questions. Each Unit shall have a marks weightage of 15.
4. The questions are to be framed keeping in view the learning outcomes of the course / paper. The standard / level of the questions to be asked should be at the level of the prescribed textbook.
5. The requirement of (scientific) calculators / log-tables / data – tables may be specified if required.

Course Objectives :

1.	To provide an understanding about the concepts of transfer unction and its evaluation.
2.	To expose the students to time response of control systems
3.	To understand the frequency response of control systems
4.	To study compensators and controllers

Course Outcomes (CO)

CO 1	Ability to define, understand various terms related to control system and evaluation of transfer function
CO 2	Ability to apply knowledge of various types of signals in time response of systems
CO 3	Ability to analyse frequency response of systems
CO 4	Ability to design compensators and controllers

Course Outcomes (CO) to Programme Outcomes (PO) mapping (scale 1: low, 2: Medium, 3: High)

	PO01	PO02	PO03	PO04	PO05	PO06	PO07	PO08	PO09	PO10	PO11	PO12
CO 1	3	3	2	1	1	1	1	-	1	3	-	3
CO 2	3	2	1	3	2	1	1	-	1	3	-	1
CO 3	3	2	1	2	3	1	1	-	1	3	-	3
CO 4	3	3	2	1	1	1	1	-	1	3	-	3

UNIT I

Control Systems: Basics & Components Introduction to basic terms, classifications & types of Control Systems, Mathematical modelling of real life systems, block diagrams & signal flow graphs. Transfer function, determination of transfer function using Block diagram reduction techniques and Mason's Gain formula. Control system components: Electrical/ Mechanical/Electromechanical/A.C./D.C. Servo Motors, Stepper Motors, Tacho Generators, Synchros, Magnetic Amplifiers, Servo Amplifiers.

UNIT II

Time: Domain Analysis of real life problems, Time domain performance specifications, transient response of first & second order systems, steady state errors and static error constants in unity feedback control systems, response with P, PI and PID controllers, limitations of time domain analysis.

UNIT III

Frequency Domain Analysis frequency domain specifications and performance of LTI systems, minimum/non minimum phase systems, Polar and inverse polar plots, Logarithmic plots (Bode plots), gain and phase margins, relative stability. Correlation with time domain performance, closed loop frequency responses from open loop response. Limitations of frequency domain analysis.

UNIT IV

Stability & Compensation Techniques Concepts, absolute, asymptotic, conditional and marginal stability, Routh–Hurwitz and Nyquist stability criterion, Root locus technique and its application. Concepts of compensation, series/parallel/ series-parallel/feedback compensation, Lag/Lead/Lag-Lead networks for compensation, compensation using P, PI, PID controllers.

Textbooks:

1. B. C. Kuo, “Automatic control system”, Prentice Hall of India, 7th edition 2001.
2. Nagrath Gopal, “Control Systems Engineering -Principles and Design” New Age Publishers

References:

1. Norman S. Nise, “Control systems engineering” John Wiley & Sons (Asia) Singapore.
2. B. S. Manke, Linear Control System, Khanna publication.
3. K. Ogata, “Modern control engineering”, Pearson 2002.
4. A. K. Jaurath , Problems And Solutions Of Control Systems: With Essential Theory (CBS Problems and Solutions Series)

Microelectronics Lab	L	P	C
		2	1

Discipline(s) / EAE / OAE	Semester	Group	Sub-group	Paper Code
ECE/EE-VDT/EC-ACT	5	PC	PC	ECC-353

Marking Scheme:
1. Teachers Continuous Evaluation: 40 marks
2. Term end Theory Examinations: 60 marks

Instructions:
1. The course objectives and course outcomes are identical to that of (Microelectronics) as this is the practical component of the corresponding theory paper.
2. The practical list shall be notified by the teacher in the first week of the class commencement under intimation to the office of the Head of Department / Institution in which the paper is being offered from the list of practicals below. Atleast 10 experiments must be performed by the students, they may be asked to do more. Atleast 5 experiments must be from the given list.

1. To study the MOS characteristics and introduction to tanner EDA software tools.
2. To design and study the DC characteristics of PMOS and NMOS.
3. To design and study the DC and AC characteristics of CMOS inverter.
4. To design and study the characteristics of CMOS NAND and NOR gate.
5. To design any Boolean function using transmission gates.
6. To design and study the characteristics of CMOS multiplexer.
7. To design and study the layout of PMOS and NMOS transistors.
8. To design and study the layout of CMOS inverter.
9. To design and study the layout of 2 I/P CMOS NAND gate
10. To design and study the layout of 2 I/P CMOS NOR gate
11. To design and study the layout of CMOS XOR gate.

Microelectronics	L	P	C
	3		3

Discipline(s) / EAE / OAE	Semester	Group	Sub-group	Paper Code
ECE/EE-VDT/EC-ACT	5	PC	PC	ECC-305

Marking Scheme:

1. Teachers Continuous Evaluation: 25 marks
2. Term end Theory Examinations: 75 marks

Instructions for paper setter:

1. There should be 9 questions in the term end examinations question paper.
2. The first (1st) question should be compulsory and cover the entire syllabus. This question should be objective, single line answers or short answer type question of total 15 marks.
3. Apart from question 1 which is compulsory, rest of the paper shall consist of 4 units as per the syllabus. Every unit shall have two questions covering the corresponding unit of the syllabus. However, the student shall be asked to attempt only one of the two questions in the unit. Individual questions may contain upto 5 sub-parts / sub-questions. Each Unit shall have a marks weightage of 15.
4. The questions are to be framed keeping in view the learning outcomes of the course / paper. The standard / level of the questions to be asked should be at the level of the prescribed textbook.
5. The requirement of (scientific) calculators / log-tables / data – tables may be specified if required.

Course Objectives :

1.	To comprehend semiconductor physics, band theory, and material behavior, demonstrating knowledge of semiconductor applications in electronic devices.
2.	To analyze and design analog and digital circuits, exhibiting skills in circuit analysis techniques for complex electronic systems.
3.	To gain practical knowledge of semiconductor fabrication processes, understanding techniques such as lithography, doping, and their impact on device performance.
4.	To use microelectronic components in designing and prototyping electronic systems, integrating devices into applications like integrated circuits, sensors, and communication devices.

Course Outcomes (CO)

CO 1	Comprehend semiconductor physics, band theory, and material behavior, demonstrating knowledge of semiconductor applications in electronic devices.
CO 2	Ability to analyze and design analog and digital circuits, exhibiting skills in circuit analysis techniques for complex electronic systems.
CO 3	Gain practical knowledge of semiconductor fabrication processes, understanding techniques such as lithography, doping, and their impact on device performance.
CO 4	Ability to use microelectronic components in designing and prototyping electronic systems, integrating devices into applications like integrated circuits, sensors, and communication devices.

Course Outcomes (CO) to Programme Outcomes (PO) mapping (scale 1: low, 2: Medium, 3: High)

	PO01	PO02	PO03	PO04	PO05	PO06	PO07	PO08	PO09	PO10	PO11	PO12
CO 1	3	3	3	2	2	1	1	-	-	2	1	2
CO 2	2	3	3	2	3	1	2	-	1	2	2	2
CO 3	2	3	3	2	3	1	2	-	1	2	2	2
CO 4	2	3	3	2	3	1	2	-	1	2	2	2

UNIT I

Introduction to Microelectronics, Overview of Microelectronics Technology, Basic IC Fabrication Processes (Oxidation, Diffusion, Ion Implantation, etc.), Cleanroom Protocols and Safety Measures. CMOS & NMOS process technology. MOS capacitor, device structure & electrical characteristics. MOS under external bias, derivation of threshold voltage equation, enhancement & depletion transistor, MOS device design equations, MOSFET capacitances. MOSFET scaling and various short channel effects, Moore's law, multi-gate MOSFETs, non-conventional MOSFET, technology nodes and ITRS.

UNIT II

CMOS inverter and its DC characteristics, Static & dynamic power dissipation. Rise time, fall time delays, noise margin. Combinational CMOS logic circuits, pass transistor and transmission gate designs, Sequential MOS logic circuits: SR latch, CMOS D latch and edge triggered flip flop. Dynamic CMOS logic circuits: Domino CMOS logic, NORA CMOS logic, Zipper, TSPC.

UNIT III

Current Mirrors and Differential Amplifiers, Operational Amplifiers (Op-Amps) Design: Ideal vs. Practical Models, Frequency Response of Op-Amps, Feedback Topologies (Voltage, Current, and Transconductance Feedback), Voltage Reference Circuits, Linear Voltage Regulators, Switching Voltage Regulators, Stability Analysis and Compensation Techniques.

Unit IV

Static RAM (SRAM) Design: 6T Cell, Read and Write Operations, Dynamic RAM (DRAM) Design: Basic Cell, Refresh Techniques, Flash Memories: NOR and NAND Architectures, Non-Volatile Memories Design: EEPROM, Ferroelectric RAM (FeRAM), MRAM, Low-Power IC Design Techniques, Analog-to-Digital Converters (ADCs), Digital-to-Analog Converters (DACs), Radio-Frequency Integrated Circuits (RFICs): Basics and Applications.

Textbooks:

1. Rabaey, J. M., Chandrakasan, A., & Nikolic, B. (2016). Digital Integrated Circuits: A Design Perspective. Pearson.
2. Razavi, B. (2016). Design of Analog CMOS Integrated Circuits. McGraw-Hill Education.
3. Weste, N. H. E., & Harris, D. (2015). CMOS VLSI Design: A Circuits and Systems Perspective. Pearson.
4. Kang, S. M., & Leblebici, Y. (2016). CMOS Digital Integrated Circuits: Analysis and Design. McGraw-Hill Education.

References:

1. Gray, P. R., Hurst, P. J., Lewis, S. H., & Meyer, R. G. (2001). Analysis and Design of Analog Integrated Circuits. Wiley.
2. Malvino, A. P., & Bates, J. A. (2012). Electronic Principles. McGraw-Hill Education.
3. Sedra, A. S., & Smith, K. C. (2014). Microelectronic Circuits. Oxford University Press.
4. Lee, T. H. (2004). The Design of CMOS Radio-Frequency Integrated Circuits. Cambridge University Press.

Transmission Lines, Waveguides and Antenna Design Lab	L	P	C
		2	1

Discipline(s) / EAE / OAE	Semester	Group	Sub-group	Paper Code
ECE/EE-VDT/EC-ACT	5	PC	PC	ECC-357

Marking Scheme:
1. Teachers Continuous Evaluation: 40 marks
2. Term end Theory Examinations: 60 marks

Instructions:
1. The course objectives and course outcomes are identical to that of (Transmission Lines, Waveguides and Antenna Design) as this is the practical component of the corresponding theory paper.
2. The practical list shall be notified by the teacher in the first week of the class commencement under intimation to the office of the Head of Department / Institution in which the paper is being offered from the list of practicals below. Atleast 10 experiments must be performed by the students, they may be asked to do more. Atleast 5 experiments must be from the given list.

1. To design and simulate a coaxial transmission line and obtain the propagation constant.
2. To design and simulate strip line and microstrip line and coplanar line and obtain the propagation constants.
3. To design and simulate a rectangular waveguide.
4. To design and simulate a circular waveguide.
5. To design and simulate a dipole antenna.
6. To design and simulate a slotted a rectangular waveguide antenna.
7. To design and simulate a leaky wave antenna using the rectangular waveguide.
8. To design and simulate a rectangular microstrip patch antenna.
9. To design and simulate a circular patch antenna.
10. To design and simulate a rectangular microstrip patch antenna array.
11. To design and simulate a circular microstrip patch antenna array.

Note: These experiments may be performed using simulation software like HFSS, CST and IE3D.

Transmission Lines, Waveguides and Antenna Design	L	P	C
	4		4

Discipline(s) / EAE / OAE	Semester	Group	Sub-group	Paper Code
ECE/EE-VDT/EC-ACT	5	PC	PC	ECC-309

Marking Scheme:
1. Teachers Continuous Evaluation: 25 marks
2. Term end Theory Examinations: 75 marks

Instructions for paper setter:
1. There should be 9 questions in the term end examinations question paper.
2. The first (1st) question should be compulsory and cover the entire syllabus. This question should be objective, single line answers or short answer type question of total 15 marks.
3. Apart from question 1 which is compulsory, rest of the paper shall consist of 4 units as per the syllabus. Every unit shall have two questions covering the corresponding unit of the syllabus. However, the student shall be asked to attempt only one of the two questions in the unit. Individual questions may contain upto 5 sub-parts / sub-questions. Each Unit shall have a marks weightage of 15.
4. The questions are to be framed keeping in view the learning outcomes of the course / paper. The standard / level of the questions to be asked should be at the level of the prescribed textbook.
5. The requirement of (scientific) calculators / log-tables / data – tables may be specified if required.

Course Objectives :

1.	To familiarise the various types of transmission lines and to deliberate the losses associated.
2.	To communicate information about waveguide concepts
3.	To impart the understanding of characteristics of different types of high frequency resonators.
4.	To impart the knowledge to define different terminologies of antenna parameters.

Course Outcomes (CO)

CO 1	To Understand the primary model of wave propagation in Transmission Lines and Analyze the various line parameters and Apply smith chart for line parameter and impedance calculations.
CO 2	Discuss the fundamental concepts of wave propagation in rectangular and circular waveguides and evaluate their characteristics.
CO 3	Understand the characteristics of resonance frequency of different types of resonator and its modes configuration.
CO 4	To describe the basic parameters of antenna and interpret to solve the radiation components

Course Outcomes (CO) to Programme Outcomes (PO) mapping (scale 1: low, 2: Medium, 3: High)

	PO01	PO02	PO03	PO04	PO05	PO06	PO07	PO08	PO09	PO10	PO11	PO12
CO 1	3	3	3	3	2	1	1	-	2	1	-	2
CO 2	3	3	3	3	2	1	1	-	2	1	-	2
CO 3	3	3	3	3	2	1	1	-	2	1	-	2
CO 4	3	3	3	3	2	1	1	-	2	1	-	2

UNIT I

Microwave Transmission Lines: Transmission-Line Equations, Solutions of Transmission-Line Equations. Reflection Coefficient, Transmission Coefficient. Standing Wave, Standing-Wave Ratio, Line Impedance, Line Admittance, Open and short circuited lines. Smith Chart Impedance Matching: Single-Stub Matching, Double-Stub Matching. Losses in transmission lines. Lines of different lengths – $\lambda/2$, $\lambda/4$, $\lambda/8$ lines.
Introduction to Microstrip transmission line.

UNIT II

Microwave Waveguides and Components:

Introduction Rectangular Waveguides: Solutions of Wave Equations in Rectangular Coordinates, TE Modes in Rectangular Waveguides, TM Modes in Rectangular Waveguides, Power Transmission in Rectangular Waveguides, Losses in Rectangular Waveguides, Excitations of Modes in Rectangular Waveguides.
Circular Waveguides: Solutions of Wave Equations in Cylindrical Coordinates, TE Modes in Circular Waveguides, TM Modes in Circular Waveguides, Excitations of Modes in Circular Waveguides.

UNIT III

Microwave Resonators: Series and Parallel Resonant Circuits: Series Resonant Circuit, Parallel Resonant Circuit, Loaded and Unloaded *Q.*
Transmission Line Resonators: Short-Circuited λ/2 line, Open-Circuited λ/2, Short-Circuited λ/4 Line; Rectangular Waveguide Cavities: Resonant Frequencies, *Q* of the TE_{10l} Mode; Circular Waveguide Cavities: Resonant Frequencies, Q of the TE_{nml} Mode. Dielectric Resonators: Resonant Frequencies, *Q* of the $TE_{01\delta}$ Mode. Excitation of Resonators: Critical Coupling, A Gap-Coupled Microstrip Resonator.

UNIT IV

Antennas: Introduction, Types of Antennas, Radiation Mechanism. Introduction monopole and dipole antenna.
Fundamental Parameters: Introduction, Radiation Pattern, Radiation Power Density, Radiation Intensity, Beamwidth, Directivity, Antenna Efficiency, Gain, Realized Gain, Beam Efficiency, Antenna Radiation Efficiency, Friis Transmission Equation and Radar Range Equation
Radiation Integrals and Auxiliary Potential Functions: The Vector Potential A for an Electric Current Source J, The Vector Potential F for A Magnetic Current Source M, Electric and Magnetic Fields for Electric (J) and Magnetic (M) Current Sources, Solution of the Inhomogeneous Vector Potential Wave Equation, Far-Field Radiation, Duality Theorem, Reciprocity Theorems

Textbook(s):
1. M. N. O. Sadiku , “Elements of Electromagnetics”, Oxford University Press 2007
2. S.Y Liao, “Microwave devices and Circuits” Pearson publications
3. D.M Pozar, “Microwave Engineering”, Wiley Publications.
4. Antenna for all Application-John D Kraus, third edition-TMH publication
5. Antenna Theory-Constantine A. Balanis -Third edition-Wiley Publication

References:
1. E. C. Jordon, K. G. Balman, “Electromagnetic Waves & Radiation System” Prentice Hall, India
2. Antennas and Wave Propagation–G. S. N. Raju (Pearson)
3. Foundations of Antenna Theory and Techniques – Vincent F. Fusco(Pearson)